IN THE CLAIMS:

1. (currently amended) A method of making transistors, the method comprising:
selectively depositing a first metal layer on a gate dielectric of a first region of a wafer and not on a gate dielectric of a second region of the wafer;
depositing a second metal layer over the gate dielectric of the second region;
forming a first gate electrode stack for a first transistor in the first region, the first gate electrode stack including a structure formed from the first metal layer;
forming a second gate electrode stack for a second transistor in the second region, the second gate electrode stack including a structure formed from the second metal layer,
wherein the method further comprises:
forming an inhibitor on the gate dielectric of the second region, wherein the inhibitor inhibits the deposition of the first metal layer on the gate dielectric of the second region.

2. (original) The method of claim 1 wherein the first transistor is a PMOS transistor and the second transistor is an NMOS transistor.

3. (original) The method of claim 1 wherein the first transistor is an NMOS transistor and the second transistor is a PMOS transistor.

4. (original) The method of claim 1 wherein:
the depositing the second metal layer further comprises depositing the second metal layer over the first metal layer in the first region;
wherein the first gate electrode stack includes a structure formed from the second metal layer over the first metal layer.

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6. (currently amended) The method of claim ~~5~~ 1 wherein the inhibitor inhibits by blocking nucleation sites on the gate dielectric of the second region.

7. (currently amended) The method of claim ~~5~~ 1 wherein the inhibitor is characterized as a self assembling monolayer.

8. (currently amended) The method of claim ~~5~~ 1 wherein the inhibitor includes an organosilane.

9. (currently amended) The method of claim ~~5~~ 1, wherein the inhibitor includes a methyl group.

10. (currently amended) The method of claim ~~5~~ 1 wherein the inhibitor includes a methacrylate based polymer.

11. (currently amended) The method of claim ~~5~~ 1 wherein the inhibitor includes a photodefinable polymer.

12. (currently amended) The method of claim ~~5~~ 1 wherein the forming an inhibitor further comprises:

selectively forming the inhibitor on the gate dielectric of the second region and not on the gate dielectric of the first region.

13. (original) The method of claim 12 wherein the selectively forming the inhibitor includes forming the inhibitor by stamping.

14. (original) The method of claim 13 wherein the selectively forming the inhibitor includes applying material of the inhibitor by print stamping.

15. (original) The method of claim 14 wherein the applying material of the inhibitor by print stamping includes stamping the wafer with a stamp mask having a layer of inhibitor material at a location on the mask corresponding to the second region.

16. (original) The method of claim 15 wherein the location on the mask is a proud portion of the mask.

17. (currently amended) The method of claim ~~5~~ 1 further comprising:
neutralizing the inhibitor after the depositing the first metal layer and prior to the depositing the second metal layer.

18. (original) The method of claim 17 wherein the neutralizing the inhibitor includes removing the inhibitor.

19. (original) The method of claim 17 wherein the neutralizing the inhibitor further includes heating the wafer at 100 C or greater.

20. (original) The method of claim 17 wherein the neutralizing the inhibitor further includes plasma treating the inhibitor.

21. (original) The method of claim 17 wherein the neutralizing the inhibitor further includes plasma etching the inhibitor.

22. (original) The method of claim 17, wherein the neutralizing the inhibitor further includes irradiating the inhibitor with ultra violet (UV) radiation.

23. (original) The method of claim 1 wherein the first metal layer includes one of tantalum silicon nitride, tantalum carbide, a metal boride, a metal silicon nitride, and a metal carbide.

24. (original) The method of claim 1 wherein the first metal layer includes one of titanium nitride, iridium, iridium oxide, ruthenium, ruthenium oxide, and tantalum nitride.

25. (original) The method of claim 1 wherein the first metal layer is selectively deposited using an atomic layer deposition (ALD) process.

26. (original) The method of claim 1 wherein the first metal layer is selectively deposited using a chemical vapor deposition (CVD) process.

27. (original) The method of claim 1 further comprising:
forming a polysilicon layer over the first metal layer in the first region and a polysilicon layer over the second metal layer in the second region;
wherein the first gate electrode stack includes a structure formed from the polysilicon layer over the first metal layer in the first region;
wherein the second gate electrode stack includes a structure formed from the polysilicon layer over the second metal layer in the second region.

28. (original) The method of claim 1 wherein the first metal layer has a first work function and the second metal layer has a second work function, the first work function is different from the second work function.

29. (original) A method of making a transistor, the method comprising:
selectively forming an inhibitor on a dielectric in a first region of a wafer and not on a dielectric of a second region of the wafer;
selectively depositing a metal layer on the dielectric of the second region, wherein the inhibitor inhibits the deposition of the metal layer on the dielectric of the first region;
forming a gate electrode stack for a transistor in the second region, the gate electrode stack including a structure formed from the metal layer.

30. (original) The method of claim 29 further comprising:
depositing a second metal layer on a dielectric of the first region;
forming a second gate electrode stack for a second transistor in the first region of the wafer, the second gate electrode stack including a structure formed from the second metal layer.

31. (original) The method of claim 30 further comprising:
neutralizing the inhibitor after the depositing the metal layer and prior to the depositing the second metal layer.

32. (original) The method of claim 29 further comprising:
neutralizing the inhibitor after the depositing the metal layer and prior to the forming the gate electrode stack.

33. (original) The method of claim 29 wherein the inhibitor includes a methyl group.

34. (original) The method of claim 29 wherein the inhibitor includes an organosilane

35. (original) The method of claim 29 wherein the inhibitor is characterized as a self assembling monolayer.

36. (original) The method of claim 29 wherein the selectively forming the inhibitor includes forming the inhibitor by stamping.

37. (original) The method of claim 29 wherein the selectively forming the inhibitor includes applying material of the inhibitor by print stamping.

38. (original) A method of making transistors, the method comprising:
selectively forming an inhibitor on a gate dielectric in a first region of a wafer and not on a gate dielectric in a second region of the wafer;
selectively depositing using an atomic layer deposition process, a first metal layer on the gate dielectric of the second region while inhibiting the deposition of the first metal layer on the gate dielectric of the first region;
depositing a second metal layer over the gate dielectric of the first region;
forming a first gate electrode stack for a first transistor in the first region, the first gate electrode stack including a structure formed from the second metal layer;
forming a second gate electrode stack for a second transistor in the second region, the second gate electrode stack including a structure formed from the first metal layer.

39. (original) The method of claim 38 further comprising:
forming source/drain regions for the first transistor and the second transistor.